REMARKS/ARGUMENTS

In response to the Examiner's final Office Action of July 5, 2005 the Applicant submits the accompanying Amendment to the claims and the below Remarks directed thereto.

Claims 1-8 as filed are currently pending in the present application. In the Amendment:

independent claim 5 is amended to omit "for performing the method" in order to clarify the recitation;

new claims 9 and 10, respectively dependent on claims 1 and 5, are added reciting that the pMOS and nMOS transistors of the non-flashing CMOS structures are driven under non-synchronized clock signals. Support for these new claims can be found at page 107, line 29-page 108, line 5 and Figs. 15 and 16 of the present application; and

claims 1-4 and 6-8 are unchanged.

It is respectfully submitted that the above amendments do not add new matter to, nor present new issues to the prosecution of, the present application.

REMARKS

35 USC 103(a) rejections

It is respectfully submitted that the subject matter of method claims 2-4 and 9 and (amended) authentication chip claims 5-8 and 10 is not taught or suggested by Park (USP 5,673,223) either taken alone or in combination with what the Examiner purports to be well known in the art, for at least the following reasons.

Regarding "well known in the art"

Despite the Applicant's repeated arguments against what the Examiner has contended as being well known in the art of semiconductors in the previous Office Actions issued in the present application, the Examiner has maintained this contention in the present final Office Action again without providing supporting documentary evidence.

The Applicant respectfully reminds the Examiner of the Examiner's obligations specified in the MPEP §2144.03 regarding the taking of official notice unsupported by documentary evidence.

These obligations require that such official notice "should only be taken by the Examiner where the facts asserted to be well known in the art are capable of instant and unquestionable demonstration as being well known." It is respectfully submitted that the to shielding of secret data by driving pMOS and nMOS transistors of a CMOS structure so that they do not present intermediate resistance simultaneously and operating conventional CMOS inverters adjacent such CMOS structures is not capable of instant and unquestionable demonstration as being well known.

Further, the obligations of the MPEP §2144.03 state that "it is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based. See *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697; *Ahlert*, 424 F.2d at 1092, 165 USPQ 421." It is respectfully submitted

that what the Examiner is purported as being well known in the art is being used as the principal evidence upon which the obviousness rejection is based.

This is because, the cited reference in Park is in no way relevant to the manipulation or shielding of secret data in CMOS structures. Rather, as previously discussed by the Applicant in response to the first Office Action, Park merely discloses a memory device and a process of storing data therein (see col. 4, line 18-col. 5, line 27 of Park). Thus, it is the Examiner's purported well known design which is being relied upon as the principal evidence.

Based on the above, if the Examiner is to maintain the current obviousness rejection, it is respectfully requested that the Examiner provide the necessary documentary evidence to support what the Examiner purports as being well known in the art as required by the MPEP §2144.03. If such evidence is not available to the Examiner, then it is respectfully requested that the Examiner withdraw the current rejection.

Regarding new claims 9 and 10

As discussed above, the Applicant has added new dependent claims 9 and 10 reciting that the pMOS and nMOS transistors of the non-flashing CMOS structures are driven under non-synchronized clock signals, as illustrated in Figs. 15 and 16 of the present application. This arrangement drives the pMOS and nMOS transistors so as not to present intermediate resistance simultaneously, which eliminates light emission during data manipulation in the CMOS structures and therefore shields the secret data (see page 107, line 16-page 108, line 14 of the present specification).

Park does not disclose such a non-flashing CMOS structure. This is because, the pMOS and nMOS transistors of the memory circuits (word line voltage generators) of Park are not driven under non-synchronized clocks. Thus, these generator circuits of Park do not constitute CMOS structures which are used for the secure manipulation of secret data.

Thus, it is respectfully submitted that the subject matter of claims 1-10 is not taught or suggested by Park either taken alone or in combination with what the Examiner purports as being well known in the art.

It is respectfully submitted that all of the Examiner's rejections have been traversed. Accordingly, it is submitted that the present application is in condition for allowance and reconsideration of the present application is respectfully requested.

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Very respectfully,

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